WHAT IS CLAIMED IS:

~~Claims~~

1. An arrangement having an electric motor (10; 10'),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function, in which arrangement

an output (A) of the microprocessor (12) can be switched over in program-controlled fashion to a high level or to a low level;

and a tapping point (19) **[sic]** of a first voltage divider (20, 22) is connected to that terminal via a resistor (17) in order to make the potential of that voltage divider tapping point (18) switchable in program-controlled fashion between at least two values by modifying that level.

2. The arrangement as defined in claim 1, in which said resistor (17) is of high-resistance configuration.

3. The arrangement as defined in claim 2, in which the value of said resistor (17) is 50 kilohms or more.

4. The arrangement as defined in one or more of claims 1 through 3, in which said output (A) of the microprocessor (12) can be switched over in program-controlled fashion to a third, high-resistance state (FIG. 4).

5. The arrangement as defined in one or more of the foregoing claims, in which the potential at the tapping point (18) of the first voltage divider (20, 22) serves to influence a parameter of the motor (10; 10').

6. The arrangement as defined in one or more of the foregoing claims, in which there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) influencing a parameter of the motor (10; 10').

7. The arrangement as defined in claim 6, in which the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

8. The arrangement as defined in claim 6 or 7, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

9. The arrangement as defined in one of more of the foregoing claims, in which the potential at the tapping point (18; 163) of the first and/or second voltage divider (20, 22; 160) defines a current limiting value (I_{ref}) for limiting the motor current (i).

10. The arrangement as defined in claim 9, having a nonvolatile memory element (14) which stores at least one time value (T_D) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

11. A method for controlling the startup of an electric motor with which a microcontroller or microprocessor, hereinafter called a microprocessor, is associated for control purposes, having the following steps:

after the motor is switched on, an acceleration time (T_S) is monitored;

during that acceleration time (T_S), the current limiting value (I_{ref}) of an arrangement for limiting the motor current (i) is set in program-controlled fashion to a first value ($I_{ref} = 1$);

when it is ascertained that the acceleration time (T_S) has expired, the current limiting value (I_{ref}) is switched over in program-controlled fashion to a second value ($I_{ref} = TST$) that is different from the first value.

12. The method as defined in claim 11, in which the second current limiting value is less than the first.

13. The method as defined in claim 11 or 12, in which, after the acceleration time (T_S) has expired, a determination is made as to whether motor current limiting is effective during a time span that exceeds a predefined time span;

and if such is the case, the current limiting value (I_{ref}) is switched over in program-controlled fashion to a third value ($I_{ref} = 0$).

14. The method as defined in one or more of claims 11 through 13, in which at least the acceleration time (T_S) is stored in a nonvolatile memory element (14) whose values can be entered and/or modified via a data bus (13, 15).

15. An arrangement for carrying out the method as defined in one or more of claims 11 through 14, in which the microprocessor (12) for program-controlled switchover of the current limiting value (I_{ref}) has at least one output (A) that can be switched over at least between a high and a low signal level and thereby influences the current limiting value (I_{ref}); and that signal level can be modified in program-controlled fashion during acceleration of the motor (10; 10').

16. The arrangement as defined in claim 15, in which the at least one output (A) can be switched over to a high-resistance state called the tristate state.

17. The arrangement as defined in claim 15 or 16, in which the output (A) serving to switch over the current limiting value is connected via a resistor (17) to the tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows, and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

18. The arrangement as defined in claim 17, in which there is provided parallel to one branch (22) of the first voltage divider (20, 22) a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows, and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

19. The arrangement as defined in claim 18, in which the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20. The arrangement as defined in claim 18 or 19, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

21. The arrangement as defined in one or more of claims 17 through 20, in which the voltage (u) at the measurement resistor (36) is filtered through a low-pass element (38, 42) before comparison with the aforesaid potential.

22. The arrangement as defined in claim 21, in which the low-pass element is configured as a first-order low-pass element (38, 42).

23. An arrangement having an electric motor (10; 10'), in particular for driving a fan (73),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function,

having a nonvolatile memory element (14) for storing at least one variable as a definition for that motor function;

and having an interface (13a), associated with the electric motor, for a data line (13) for transferring that at least one variable to and/or from the nonvolatile memory element (14).

24. The arrangement as defined in claim 23, in which the microprocessor (12) is connected (lines 210, 226) to the interface (13a) for the data line (13);

and the transfer of data from and/or to the nonvolatile memory element (14) is accomplished via the microprocessor (12).

25. The arrangement as defined in claim 23 or 24, in which the data line is configured as a serial data bus (13, 210, 226).

26. The arrangement as defined in claim 25, in which there is associated with the microprocessor (12) a stored directory (280) which contains, for objects that are transferable via the data line (13, 210, 226), predefined parameters (286, 288, 290) for the transfer of those objects.

27. The arrangement as defined in claim 26, in which the stored directory (280) contains data (286) as to the length of transferable objects.

28. The arrangement as defined in claim 26 or 27, in which the stored directory (280) contains data (288) as to whether the relevant object is intended for storage in the nonvolatile memory element (14) or in a volatile memory element (330).

29. The arrangement as defined in one or more of claims 26 through 28, in which the stored directory (280) contains data (290) as to the address of the object in a memory element (14, 330).

30. The arrangement as defined in one or more of claims 23 through 29, in which the stored directory (280) is stored in nonvolatile and, in particular, permanent fashion in a memory (336) associated with the microprocessor (12).

31. The arrangement as defined in claim 30, in which the stored directory (280) is a hardware component of the microprocessor (12).

32. The arrangement as defined in one or more of claims 23 through 31, in which at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in a volatile memory (330) associated with the microprocessor (12).

33. The arrangement as defined in one or more of claims 23 through 32, in which the nonvolatile memory element (14) is connected via a serial bus (15) to the microprocessor (12).

34. The arrangement as defined in claim 33, in which the nonvolatile memory element (14) is connected via a line (CS) to the microprocessor (12) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).

35. The arrangement as defined in one or more of claims 23 through 34, in which the microprocessor (12) has a predefined memory element (332) for storing an address (FIG. 17: 242; FIG. 18: 254) conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparison arrangement for comparing those two addresses.

36. The arrangement as defined in one or more of claims 23 through 35, in which a memory element (332) for storing a variable (FIGS. 18, 19: 246; FIG. 18: 254) that characterizes an object to be transferred is associated with the microprocessor (12); and by way of that variable, at least one characteristic (286, 288, 290) of that object can be taken, for processing thereof, from a directory (280) stored in the arrangement.

37. The arrangement as defined in claim 36, in which the characteristic is the length (286) of that object.

38. The arrangement as defined in claim 36 or 37, in which the characteristic is the hardware address (288, 290) of that object.

39. Use of an arrangement and/or a method as defined in one or more of the foregoing claims in a motor (10; 10') that drives a fan (73; 340).

40. The use as defined in claim 39, in which the fan is an equipment fan (340A, 340B, 240C).

[amended Claims]

PCT/EP99/03992
July 13, 2000
P61.12PCT215
PCT-3037

Claims

1. An arrangement having an electric motor (10; 10'),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function,

in which arrangement an output (A) of the microprocessor (12) can be switched over in program-controlled fashion to a high level or to a low level;

and a tapping point (19) [sic] of a first voltage divider (20, 22) is connected to that terminal via a resistor (17) in order to make the potential of that voltage divider tapping point (18) switchable in program-controlled fashion between at least two values by modifying that level, and by way of that potential to influence a parameter of the motor (10; 10').

2. The arrangement as defined in claim 1, in which the parameter is a current limiting value (Iref) for limiting the motor current (i) of the electric motor (10; 10').

3. The arrangement as defined in claim 1 or 2, in which said resistor (17) is of high-resistance configuration.

4. The arrangement as defined in claim 3, in which the value of said resistor (17) is 50 kilohm or more.

5. The arrangement as defined in one or more of claims 1 through 4, in which said output (A) of the microprocessor (12) can be switched over in program-controlled fashion to a third, high-resistance state (FIG. 4).

6. The arrangement as defined in one or more of the foregoing claims, in which there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) influencing the parameter of the motor (10; 10').

7. The arrangement as defined in claim 6, in which the second voltage divider (160) has a higher resistance as compared to the resistance value of the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

8. The arrangement as defined in claim 6 or 7, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

9. The arrangement as defined in one of more of claims 6 through 8, in which the potential at the tapping point (163) of the second voltage divider (160) defines a current limiting value (Iref) for limiting the motor current (i) of the electric motor (10; 10').

10. The arrangement as defined in claim 2 or 9, having a nonvolatile memory element (14) which serves to store at least one time value (TD) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

11. A method for controlling the startup of an electric motor with which a microcontroller or microprocessor, hereinafter called a microprocessor, a nonvolatile memory element (14), a data bus (13, 15), and an arrangement for limiting the motor current (i) are associated for control purposes, the method having the following steps:

an acceleration time (TS) is stored via the data bus (13, 15) in the nonvolatile memory element (14);

after the motor is switched on, that acceleration time (TS) is monitored;

during that acceleration time (TS), the current limiting value (Iref) of the arrangement for limiting the motor current (i) is set in program-controlled fashion to a first value (Iref = 1);

when it is ascertained that the acceleration time (TS) has expired, the current limiting value (Iref) is switched over in program-

controlled fashion to a second value (Iref = TST) that is different from the first value.

12. The method as defined in claim 11, in which the second current limiting value is less than the first.

13. The method as defined in claim 11 or 12, in which, after the acceleration time (TS) has expired, a determination is made as to whether motor current limiting is effective during a time span that exceeds a predefined time span;

and if such is the case, the current limiting value (Iref) is switched over in program-controlled fashion to a third value (Iref = 0).

14. An arrangement for carrying out the method as defined in one or more of claims 11 through 13, in which the microprocessor (12) for program-controlled switchover of the current limiting value (Iref) has at least one output (A) that can be switched over at least between a high and a low signal level and thereby influences the current limiting value (Iref);

and that signal level can be modified in program-controlled fashion during acceleration of the motor (10; 10').

15. The arrangement as defined in claim 14, in which the at least one output (A) can be switched over to a high-resistance state called the tristate state.

16. The arrangement as defined in claim 14 or 15, in which the output (A) serving to switch over the current limiting value is connected via a resistor (17) to the tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

17. The arrangement as defined in claim 16, in which there is provided parallel to one branch (22) of the first voltage divider (20, 22) a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and the motor current (i) being interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

18. The arrangement as defined in claim 17, in which a comparator (28) is provided for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows.

19. The arrangement as defined in claim 17 or 18, in which the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20. The arrangement as defined in one or more of claims 17 through 19, in which the voltage division ratio of the second voltage divider (60) is designed so that when the potential at its tapping point (163) is used as a comparison potential, the result is a lower value for that comparison potential.

21. The arrangement as defined in one or more of claims 16 through 20, in which the voltage (u) at the measurement resistor (36) is filtered through a low-pass element (38, 42) before comparison with the aforesaid comparison potential.

22. The arrangement as defined in claim 21, in which the low-pass element is configured as a first-order low-pass element (38, 42).

23. An arrangement having an electric motor (10; 10'), in particular for driving a fan (73),

having a microcontroller (12) or microprocessor, hereinafter simply called a microprocessor, for influencing at least one motor function, there being associated with that microprocessor (12) a volatile memory element (330) and a nonvolatile memory element (14), which memory elements being configured for storing at least one object as a definition for that motor function;

further having an interface (13a), associated with the electric motor, for a data line (13; 210, 226) for transferring that at least one object to and/or from a memory element (14, 330),

and having a stored directory (280), associated with the microprocessor (12), which contains, for objects that are transferable via the data line (13, 210, 226), predefined parameters (286, 288, 290) for the transfer of those objects.

24. The arrangement as defined in claim 23, in which the stored directory (280) contains data (286) as to the length of transferable objects.

25. The arrangement as defined in claim 23 or 24, in which the stored directory (280) contains data (288) as to whether the relevant object is intended for storage in the nonvolatile memory element (14) or in a volatile memory element (330).

26. The arrangement as defined in one or more of claims 23 through 25, in which the stored directory (280) contains data (290) as to the address of the object in a memory element (14, 330).

27. The arrangement as defined in one or more of claims 23 through 26, in which the stored directory (280) is stored in nonvolatile and, in particular, permanent fashion in a memory (336) associated with the microprocessor (12).

28. The arrangement as defined in claim 27, in which the stored directory (280) is a hardware component of the microprocessor (12).

29. The arrangement as defined in one or more of claims 23 through 28, in which the microprocessor (12) is connected to the interface (13a) for the data line (13);

and the transfer of objects from and/or to the nonvolatile memory element (14) is accomplished via the microprocessor (12).

30. The arrangement as defined in one or more of claims 23 through 29, in which the data line is configured as a serial data bus (13, 210, 226).

31. The arrangement as defined in one or more of claims 23 through 30, in which at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in the volatile memory (330) associated with the microprocessor (12).

32. The arrangement as defined in one or more of claims 23 through 31, in which the nonvolatile memory element (14) is connected via a line (CS) to the microprocessor (12) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).

33. The arrangement as defined in one or more of claims 23 through 32, in which the microprocessor (12) has a predefined memory element (332) for storing an address (FIG. 17: 242; FIG. 18: 254) conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparison arrangement for comparing those two addresses.

34. The arrangement as defined in one or more of claims 23 through 33, in which a memory element (332) for storing a variable (FIGS. 18, 19: 246; FIG. 18: 254) that characterizes an object to be transferred is associated with the microprocessor (12);

and by way of that variable, at least one characteristic (286, 288, 290) of that object can be taken, for processing thereof, from a directory (280) stored in the arrangement.

35. The arrangement as defined in claim 34, in which the characteristic is the length (286) of that object.

36. The arrangement as defined in claim 34 or 35, in which the characteristic is the hardware address (288, 290) of that object.

37. Use of an arrangement and/or a method as defined in one or more of the foregoing claims in a motor (10; 10') that drives a fan (73; 340).

38. The use as defined in claim 37, in which the fan is an equipment fan (340A, 340B, 240C).